

The LS3954A is a Low Noise, Low Drift, Monolithic Dual N-Channel JFET

The LS3954A family are matched JFET pairs for differential amplifiers. The LS3954A family of general purpose JFETs is characterized for low and medium frequency differential amplifiers requiring low offset voltage, drift, noise and capacitance

The LS3954A family exhibits low capacitance - 6pF max and a spot noise figure of - 0.5dB max. The part offers a superior tracking ability.

The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LS3954A Applications:

- Wideband Differential Amps
- High Input Impedance Amplifiers

FEATURES

LOW DRIFT	$ \Delta V_{GS1-2} / \Delta T = 5\mu\text{V}/^\circ\text{C max.}$
LOW LEAKAGE	$I_G = 20\text{pA TYP.}$
LOW NOISE	$e_n = 10\text{nV}/\sqrt{\text{Hz}} \text{ TYP.}$

ABSOLUTE MAXIMUM RATINGS @ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+150°C

Maximum Voltage and Current for Each Transistor – Note 1

$-V_{GSS}$	Gate Voltage to Drain or Source	60V
$-V_{DSO}$	Drain to Source Voltage	60V
$-I_{G(f)}$	Gate Forward Current	50mA

Maximum Power Dissipation

Device Dissipation @ Free Air – Total	400mW @ 25°C
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MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED

SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$ V_{GS1-2} / T \text{ max.}$	DRIFT VS. TEMPERATURE	5	$\mu\text{V}/^\circ\text{C}$	$V_{DG}=20\text{V}, I_D=200\mu\text{A}$ $T_A=-55^\circ\text{C to }+125^\circ\text{C}$
$ V_{GS1-2} \text{ max.}$	OFFSET VOLTAGE	5	mV	$V_{DG}=20\text{V}, I_D=200\mu\text{A}$

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

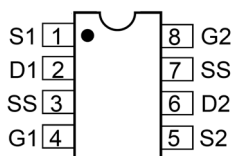
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	60	--	--	V	$V_{DS} = 0$ $I_D=1\mu\text{A}$
BV_{GGO}	Gate-To-Gate Breakdown	60	--	--	V	$I_G = 1\text{nA}$ $I_D = 0$ $I_S = 0$
TRANSCONDUCTANCE						
Y_{fss}	Full Conduction	1000	2000	3000	μmho	$V_{DG} = 20\text{V}$ $V_{GS} = 0\text{V}$ $f = 1\text{kHz}$
Y_{fs}	Typical Operation	500	700	1000	μmho	$V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$
$ Y_{FS1-2} / Y_{FS} $	Mismatch	--	0.6	3	%	
DRAIN CURRENT						
I_{DSS}	Full Conduction	0.5	2	5	mA	$V_{DG} = 20\text{V}$ $V_{GS} = 0\text{V}$
$ I_{DSS1-2} / I_{DSS} $	Mismatch at Full Conduction	--	1	5	%	
GATE VOLTAGE						
$V_{GS(off)}$ or V_p	Pinchoff voltage	1	2	4.5	V	$V_{DS} = 20\text{V}$ $I_D = 1\text{nA}$
$V_{GS(on)}$	Operating Range	0.5	--	4	V	$V_{DS} = 20\text{V}$ $I_D = 200\mu\text{A}$
GATE CURRENT						
$-I_G$	Operating	--	20	50	pA	$V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$
$-I_G$	High Temperature	--	--	50	nA	$T_A = +125^\circ\text{C}$
$-I_G$	Reduced V_{DG}	--	5	--	pA	$V_{DG} = 10\text{V}$ $I_D = 200\mu\text{A}$
$-I_{GSS}$	At Full Conduction	--	--	100	pA	$V_{DG} = 20\text{V}$ $V_{DS} = 0$
OUTPUT CONDUCTANCE						
Y_{OSS}	Full Conduction	--	--	5	μmho	$V_{DG} = 20\text{V}$ $V_{GS} = 0\text{V}$
Y_{OS}	Operating	--	0.1	1	μmho	$V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$
$ Y_{OS1-2} $	Differential	--	0.01	0.1	μmho	
COMMON MODE REJECTION						
CMR	$-20 \log V_{GS1-2} / V_{DS} $	--	100	--	dB	$\Delta V_{DS} = 10 \text{ to } 20\text{V}$ $I_D = 200\mu\text{A}$
CMR	$-20 \log V_{GS1-2} / V_{DS} $	--	75	--	dB	$\Delta V_{DS} = 5 \text{ to } 10\text{V}$ $I_D = 200\mu\text{A}$
NOISE						
NF	Figure	--	--	0.5	dB	$V_{DS} = 20\text{V}$ $V_{GS} = 0\text{V}$ $R_G = 10\text{M}\Omega$ $f = 100\text{Hz}$ $\text{NBW} = 6\text{Hz}$
e_n	Voltage	--	--	15	nV/√Hz	$V_{DS} = 20\text{V}$ $I_D = 200\mu\text{A}$ $f = 10\text{Hz}$ $\text{NBW} = 1\text{Hz}$
CAPACITANCE						
C_{ISS}	Input	--	--	6	pF	$V_{DS} = 20\text{V}$ $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
C_{RSS}	Reverse Transfer	--	--	2	pF	
C_{DD}	Drain-to-Drain	--	0.1	--	pF	$V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

LS3954A in PDIP / SOIC
LS3954A available as bare die
Please contact [Micross](http://www.micross.com) for full package and die dimensions

PDIP / SOIC (Top View)



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